

PTO-1449 (Modified)		ATTY. DOCKET NO. RA001C	SERIAL NUMBER 09/510,213
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		FILING DATE FEBRUARY 22, 2000	GROUP ART UNIT 2781

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>AA</i>	4,630,193	Dec. 16, 1986	Kris	—	—	
<i>AA</i>	4,710,904	Dec. 1, 1987	Suzuki	—	—	
<i>AA</i>	4,739,502	Apr. 19, 1988	Nozaki	—	—	
<i>AA</i>	4,905,201	Feb. 27, 1990	Ohira et al.	—	—	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>AA</i>	European Search Report for EPO Patent Application No. 00 10 0018
<i>AA</i>	European Search Report for EPO Patent Application No. 00 10 822

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AA	4,330,852	May 18, 1982	Redwine et al.	—	—	
AA	4,703,418	Oct. 27, 1987	James	—	—	
AA	4,785,394	Nov. 15, 1988	Fischer	—	—	
AA	4,726,021	Feb. 16, 1988	Horiguchi et al.	—	—	
AA	4,870,562	Sept. 26, 1989	Kimoto et al.	—	—	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
AA	S56-82961	July 7, 1981	Japan	—	—	YES
AA	S57-14922	Jan. 26, 1982	Japan	—	—	YES
AA	Sho 60-80193	May 8, 1983	Japan	—	—	YES
AA	Sho 60-55459	Mar. 30, 1985	Japan	—	—	YES
AA	S61-72350	April 14, 1986	Japan	—	—	YES
AA	S63-142445	June 14, 1988	Japan	—	—	YES
AA	B63-46864	Sept. 19, 1988	Japan	—	—	YES
AA	S64-29951	Jan. 31, 1989	Japan	—	—	YES

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AA	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
AA	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
AA	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
AA	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
AA	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

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AA	4,845,670	Jul. 4, 1989	Nishimoto et al.	—	—	
BB	4,509,142	Apr. 2, 1985	Childers	—	—	
AA	4,183,095	Jan. 8, 1980	Ward	—	—	
AA	4,685,088	Aug. 4, 1987	Ianucci	—	—	

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AA	0 246 767 /	April 28, 1987	EPO	—	—	
AA	0 334 552	Mar. 16, 1989	EPO	—	—	
AA	0 276 871 /	Jan. 29, 1988	EPO	—	—	

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AA	European Search Report for EPO Patent Application No. 00 101 1832
AA	European Search Report for EPO Patent Application No. 89 30 2613
AA	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
AA	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
AA	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
AA	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
AA	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
AA	JEDEC Standard No. 21C

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>GA</i>	4,754,433	06/28/88	Chin et al.	—	—	
<i>GA</i>	5,023,488	06/11/91	Gunning	—	—	
<i>GA</i>	4,920,486	04/24/90	Nielson	—	—	
<i>GA</i>	4,719,602	01/12/88	Haq et al.	—	—	
<i>GA</i>	4,263,650	04/21/81	Bennet et al.	—	—	
<i>GA</i>	3,771,145	11/06/73	Wiener	—	—	
<i>GA</i>	3,691,534	09/12/72	Varadi et al	—	—	
<i>GA</i>	3,969,706	07/13/76	Proebsting et al.	—	—	

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<i>GA 1</i>	M. Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with on-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987)
<i>GA 2</i>	S Watanabe et. al., "An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)

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U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		APPLICANT(S) FARMWALD ET AL.		
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RA	4,766,536	8 07/23/88	Wilson, Jr. et al.	—	—	
RA	4,998,262	03/05/91	Wiggers	—	—	
RA	4,747,079	5 03/24/88	Yamaguchi	—	—	
RA	4,649,511	03/10/87	Gdula	—	—	
RA	4,757,473	07/12/88	Kurihara et al.	—	—	
RA	4,792,926	12/20/88	Roberts	—	—	
RA	4,811,202	03/07/89	Schabowski	—	—	
RA	4,860,198	8 07/22/89	Takenaka	—	—	

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MM	4,445,204	04/24/84	Nishiguchi	—	—	
MM	4,821,226	04/11/89	Christopher et al.	—	—	
MM	4,882,712	11/21/89	Ohno et. al.	—	—	
MM	4,951,251	08/21/90	Yamaguchi et al.	—	—	
MM	4,928,265	12/29/92 05/19/90	Beigle et al. Higuchi et al.	—	—	
MM	5,107,465	04/21/92	Fung et al.	—	—	
MM	5,206,833	04/27/93	Lee	—	—	
MM	4,953,128	08/28/90	Kawai et al.	—	—	
MM	5,140,688	08/18/92	White et al.	—	—	
MM	5,018,111	05/21/91	Madland	—	—	
MM	4,734,880	03/29/88	Collins	—	—	
MM	4,183,095	01/08/80	Ward	—	—	
MM	4,975,872	12/04/90	Zaiki	—	—	

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MM	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
MM	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
AA	5,016,226	05/14/91	Hiwada et al.	—	—	
AA	5,109,498	04/28/92	Kamiya et al.	—	—	
AA	4,807,189	02/21/89	Pinkham et al.	—	—	
AA	4,092,665	05/30/78	Saran	—	—	
AA	4,799,199	01/17/89	Scales, III et al.	—	—	
AA	5,142,637	09/25/92	Harlin et al.	—	—	
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AA	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
AA	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
AA	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
AA	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol. 93, no. 1622, pp. 1243-4 (Dec. 87)
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AA	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
AA	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE International Solid State Circuits Conference, (Feb. 1989)

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
JA	5,016,226	05/14/91	Hiwada et al.	—	—	
JA	4,954,987	09/04/90	Auvinen et al.	—	—	
JA	4,675,850	06/23/87	Kumanoya et al.	—	—	
JA	4,788,667	11/29/88	Nakano et al.	—	—	
JA	4,945,516	07/31/90	Kashiyama	—	—	
JA	4,937,734	06/26/90	Bechtolsheim	—	—	
JA	4,845,664	07/04/89	Aichelmann, Jr. et al.	—	—	
JA	4,920,483	04/24/90	Pogue et al.	—	—	
JA	4,680,738	07/14/87	Tam	—	—	

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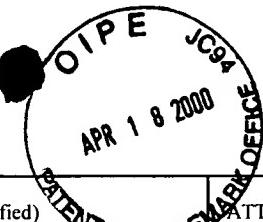
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JA	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
JA	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
JA	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
JA	M. Bazes et. al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
JA	R. Schmidt, "A memory Control Chip for Formatting Data into Blocks Suitable for Video Applications", IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1989)
JA	D. K. Morgan "The CVAX CMCTL - A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988)
JA	T.C. Poon et. al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987)
JA	E.H. Frank "The SBUS: Sun's High Performance System Bus for RISC Workstations" Sun Microsystems Inc. 1990
JA	K. Numata et. al. "New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989)

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JA	5,083,296	01/21/92	Hara et al.	—	—	
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JA	4,970,418	11/13/90	Masterson	—	—	
JA	5,361,277	11/01/94	Grover	—	—	
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